PATENT
Attorney Docket No. H1130

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Bin Yu et al.	)	Group Art Unit: 2822
	)	
Serial No.: 10/614,177	)	Examiner: K. Rose
	)	
Filed: July 8, 2003	)	
	)	
For: FLASH MEMORY DEVICE	)	
	)	

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief – Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

This Appeal Brief is submitted in response to the rejection mailed February 10, 2006 and in support of the Notice of Appeal filed May 5, 2006.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Spansion LLC.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-9, 14 and 17-22 are pending in this application. Claims 10-13, 15 and 16 have been previously canceled without prejudice or disclaimer. Claims 1-9, 14 and 17-22 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the Final Office Action mailed February 10, 2006.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Each of the independent claims involved in this appeal is recited below, followed in parenthesis by examples of where support can be found in the specification and drawings for the claimed subject matter. In addition, each dependent claim argued separately below is also summarized.

Claim 1 recites: A memory device, comprising: a substrate (page 4, paragraph 23, Fig. 1, 110); an insulating layer formed on the substrate (page 4, paragraph 23; Fig. 1, 120); a fin structure formed on the insulating layer, the fin structure having a first and second side surface and a top surface (page 5, paragraph 27; Fig. 2A, 210); a dielectric cap formed over the top surface of the fin structure (page 3, paragraph 27; Fig. 3, 140); a first spacer formed adjacent the first side surface, the first spacer acting as a first floating gate for the memory device (page 6, paragraph 30; Fig. 4, 410); a second spacer formed adjacent the second side surface, the second

spacer acting as a second floating gate for the memory device (page 6, paragraph 30; Fig. 4, 420); a gate dielectric layer formed on the first and second spacers and over the dielectric cap, the gate dielectric layer contacting the insulating layer and acting as an inter-gate dielectric for the memory device (page 6, paragraph 31; Fig. 5, 510); a first gate contacting the insulating layer and disposed on a first side of the fin (page 8, paragraph 36; Fig. 8, 810); and a second gate contacting the insulating layer and disposed on a second side of the fin opposite the first side, wherein the first and second gates are electrically isolated from each other (page 8, paragraphs 36 and 38; Fig. 8, 820).

Claim 6 recites: The memory device of claim 1, wherein each of the first and second spacers comprise polysilicon and have a width ranging from about 100 Å to about 500 Å (page 6, paragraph 30).

Claim 9 recites: The memory device of claim 8, wherein the fin structure has a width ranging from about 100 Å to about 1000 Å (page 5, paragraph 27).

Claim 14 recites: A non-volatile memory device, comprising: a substrate (page 4, paragraph 23; Fig. 1, 110); an insulating layer formed on the substrate(page 4, paragraph 23; Fig. 1, 120); a conductive fin formed on the insulating layer, the conductive fin having first and second side surfaces and a top surface (page 5, paragraph 27; Fig. 2A, 210); an oxide layer formed on the first and second side surfaces of the conductive fin (pages 5-6, paragraph 29; Fig. 3, 310); a dielectric cap formed on the top surface of the conductive fin (page 3, paragraph 27;

Fig. 3, 140); a first spacer formed adjacent the first side surface of the fin, the first spacer acting as a first floating gate electrode (page 6, paragraph 30; Fig. 4, 410); a first gate formed on the insulating layer, the first gate acting as a first control gate for the non-volatile memory device (page 8, paragraph 36; Fig. 8, 810); a second spacer formed adjacent the second side surface of the fin, the second spacer acting as a second floating gate electrode (page 6, paragraph 30; Fig. 4, 420); a second gate formed on the insulating layer, the second gate acting as a second control gate for the non-volatile memory device (page 8, paragraph 36; Fig. 8, 820), wherein the first and second gates are formed on opposite sides of the conductive fin and are electrically isolated from each other (page 8, paragraph 38); and an inter-gate dielectric formed between the first spacer and the first gate, between the second spacer and the second gate and over the dielectric cap, wherein the inter-gate dielectric contacts the insulating layer (page 6, paragraph 31; Fig. 5, 510).

Claim 21 recites: A memory device, comprising: a substrate (page 4, paragraph 23; Fig. 1, 110); an insulating layer formed on the substrate (page 4, paragraph 23; Fig. 1, 120); a fin structure formed on the insulating layer, the fin structure having a first and second side surface and a top surface (page 5, paragraph 27; Fig. 2A, 210); an oxide layer having a width ranging from about 10 Å to about 100 Å formed on the first and second side surfaces of the fin structure, the oxide layer acting as a tunnel oxide layer for the memory device (pages 5-6, paragraph 29; Fig. 3, 310); a first spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the first side surface of the fin structure, the first spacer acting as a first floating gate for the memory device (page 6, paragraph 30; page 4, 410); a second spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the second side surface of the fin structure, the

second spacer acting as a second floating gate for the memory device (page 6, paragraph 30, Fig. 4, 420); a gate dielectric layer formed on the first and second spacers and over the top surface of the fin structure (page 6, paragraph 31; Fig. 5, 510); a first gate contacting the insulating layer and disposed on a first side of the fin structure (page 8, paragraph 36; Fig. 8, 810); a second gate contacting the insulating layer and disposed on a second side of the fin structure opposite the first side (page 8, paragraph 36, Fig. 8, 820), wherein the first and second gates are electrically isolated from each other (page 8, paragraph 38); a source region formed on the insulating layer adjacent a first end of the fin structure (page 5, paragraph 28; Fig. 2B, 220); and a drain region formed on the insulating layer adjacent a second end of the fin structure opposite the first end (page 5, paragraph 28; Fig. 2B, 220).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-9, 14 and 17-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Acovic et al. (U.S. Patent No. 5,411,905; hereinafter Acovic) in view of Fried et al. (U.S. Patent Publication No. 2003/0178670; hereinafter Fried).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 103 based on Acovic in view of Fried

1. Claims 1-5, 7, 8, 14 and 18-20

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual

basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

With these principles in mind, claim 1 recites a memory device that includes a substrate; an insulating layer formed on the substrate; a fin structure formed on the insulating layer, the fin structure having a first and second side surface and a top surface; a first spacer formed adjacent the first side surface, the first spacer acting as a first floating gate for the memory device; and a second spacer formed adjacent the second side surface, the second spacer acting as a second floating gate for the memory device.

Claim 1 also recites a dielectric cap formed over the top surface of the fin structure and a gate dielectric layer formed on the first and second spacers and over the dielectric cap, the gate dielectric layer contacting the insulating layer and acting as an inter-gate dielectric for the memory device. The Final Office Action states that layer 10 of Acovic is equivalent to the claimed insulating layer and that ONO layer 24 of Acovic is equivalent to the claimed gate dielectric layer (Final Office Action – page 2). The Final Office Action, however, admits that ONO layer 24 of Acovic does not contact insulating layer 10, as required by claim 1 (Final Office Action – page 3). The Final Office Action, however, states that Fried discloses a FinFET that includes an insulating layer 99, a fin 100, first and second spacers 115 and a gate dielectric layer 116 (Final Office Action – page 3). The Final Office Action further states that gate dielectric layer 116 contacts the insulating layer 99. Fried may disclose that floating gate isolation layer 116 contacts insulator 99 and that an oxide shape 102 is formed over fin 100 (Fried – Fig. 7). Fried, however, does not disclose that gate isolation layer 116 is formed over the top surface of a dielectric cap formed over fin 100, as required by claim 1. In contrast, Fried discloses that gate isolation layer 116 abuts oxide shape 102 (see Fried – Figs. 8 and 10). Fried does not disclose that gate isolation layer 116 is formed over oxide shape 102, as required by claim 1.

Therefore, as a factual matter, the combination of Acovic and Fried cannot be fairly combined to disclose a gate dielectric layer that is both formed over a dielectric cap (formed over the top surface of a fin structure) and contacts an insulating layer, as required by claim 1.

In response to similar arguments made in the previous response, the Final Office Action states that the Acovic reference was used to disclose a gate dielectric layer 24 formed over a

dielectric cap and the Fried reference was used to disclose a gate dielectric layer 115 contacting an insulating layer (Final Office Action – page 6). While Acovic and Fried may disclose such features, Appellants assert that combining portions of ONO layer 24 of Acovic and gate isolation layer 116 of Fried to somehow arrive at the claimed gate dielectric layer amounts to an impermissible piecemeal approach to combining portions of each reference. For example, claim 1 recites a gate dielectric layer that is formed on the first and second spacers and over the dielectric cap, the gate dielectric layer contacting the insulating layer. Combining a portion of ONO layer 24 with a portion of gate isolation layer 115 amounts to a retrospective assessment of Appellants' claim 1 and then modifying various portions of the references to arrive at the claimed gate dielectric layer. Appellants assert that such a combination and subsequent modification of the combined references would not be obvious absent impermissible hindsight based on Appellants' disclosure.

Claim 1 also recites a first gate contacting the insulating layer and disposed on a first side of the fin and a second gate contacting the insulating layer and disposed on a second side of the fin opposite the first side. The Final Office Action admits that Acovic does not disclose the claimed first and second gates that contact an insulating layer (Final Office Action – page 3). The Final Office Action, however, states that it would have been obvious to modify the device of Acovic by having the control gate contact the insulating layer for electrical isolation from other surrounding structures as taught by Fried (Final Office Action – page 3). Initially, Appellants note that Fried does not disclose or suggest first and second gates that are electrically isolated from each other, as required by claim 1. Fried, in contrast, discloses a single control gate 120 (Fried – Fig. 8). Therefore, Appellants assert that Fried cannot be fairly construed as providing

motivation for modifying Acovic to include first and second gates that contact an insulating layer, as required by claim 1.

In response to similar arguments made in the previous response, the Final Office Action states that Acovic discloses first and second gates that are electrically isolated from each other and Fried discloses a gate that contacts an insulating layer. Appellants again assert that the combining and modifying portions of these references to read on the claimed first and second gates amounts to an impermissible piecemeal approach to combining portions of each reference. For example, claim 1 recites a first gate contacting the insulating layer and a second gate contacting the insulating layer, wherein the first and second gates are electrically isolated from each other. Neither reference discloses such first and second gates. Appellants assert that combining a portion of the single gate 120 of Fried with the multiple control gates 26 of Acovic amounts to a retrospective assessment of Appellants' claim 1 followed by a combination and subsequent modification of various portions of the references to arrive at the claimed first and second gates. Appellants assert that such a combination and subsequent modification of the combined references would not be obvious absent impermissible hindsight based on Appellants' disclosure.

For at least the reasons discussed above, Appellants assert that the combination of Acovic and Fried cannot be fairly construed to disclose or suggest each of the features of claim 1.

In addition, even if, for the sake of argument, the combination of Acovic and Fried could be fairly construed to disclose or suggest each of the features of claim 1, Appellants assert that that the motivation to combine Acovic and Fried does not satisfy the requirements of 35 U.S.C. § 103.

For example, the Final Office Action states that it would have been obvious to one of ordinary skill in the art to modify the device of Acovic "by having the gate dielectric layer and control gate to contact the insulating layer for electrical isolation from other surrounding structures as taught by Fried" (Final Office Action – page 3). Appellants note that no portion of either reference is pointed to as providing objective motivation for the combination. Appellants further note that the alleged motivation for combining these disclosures is merely a conclusory statement providing an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 1 under 35 U.S.C. § 103 based on Acovic and Fried is improper. Accordingly, reversal of the rejection of claims 1-5, 7, 8, 14 and 18-20 is respectfully requested.

2. Claims 6 and 17

Claim 6 recites that each of the first and second spacers comprises polysilicon and has a width ranging from about 100 Å to about 500 Å. The Final Office Action admits that neither Acovic nor Fried discloses this feature (Final Office Action – page 3). The Final Office Action, however, states that where the general conditions of a claim is disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art and relies on In re Aller for support (Final Office Action – page 4). Appellants respectfully disagree.

Acovic discloses forming a floating gate structure 22 that extends from the right side of one silicon structure 12 to the left side of an adjacent silicon structure 12 (Acovic – Fig. 2). Acovic is totally silent with respect to the width of this floating gate 22 that extends laterally

from the side of one fin structure 12 to the side of the adjacent fin structure 12 (Acovic – Fig. 2). Fried is also totally silent with respect to the width of floating gates 115. Appellants assert that absent some disclosure in Acovic or Fried with respect to the width of floating gate 22 or floating gate 115, the combination of Acovic and Fried cannot be fairly construed to suggest a floating gate that has a particular width ranging from about 100 Å to about 500 Å, as required by claim 6. In addition, the mere allegation that the claimed feature involves only routine skill in the art, without some supporting disclosure with respect to the width of floating gate 22 in Acovic or floating gate 115 in Fried, does not satisfy the requirements of 35 U.S.C. § 103.

In response to similar arguments made in the previous response, the Final Office Action states that the specification contains no disclosure as to the either the critical nature of the claimed dimensions or any unexpected results arising therefrom (Final Office Action – page 5). The Final Office Action further states that where patentability is based on particular chosen dimensions, the applicant must show that the chosen dimensions are critical and points to In re Woodruff for support (Final Office Action – page 6). Appellants respectfully disagree.

Initially, Appellants note that there is no requirement under 35 U.S.C. § 103 that a particular claim feature be "critical" in order for that claim to be patentable over the prior art. As discussed above, rejections based on 35 U.S.C. § 103 must rest on a factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 177-78 (CCPA 1967). In making such a rejection, the Examiner has the initial duty of supplying the requisite factual basis and may not, because of doubts that the invention is patentable, resort to speculation, unfounded assumptions, or hindsight reconstruction to supply deficiencies in the factual basis. Id.

In the present case, the Final Office Action has not advanced any factual basis as to why it

would have been obvious to modify the combination of Acovic and Fried to read on the feature discussed above. Instead, the Final Office Action attempts to overcome the deficiencies in the combination of Acovic and Fried by resorting to mechanical or per se rules of obviousness, such as that allegedly established by In re Aller. Such per se rules do not exist, however, and the reliance thereon to establish obviousness under 35 U.S.C. § 103 is improper. See In re Ochiai, 71 F.3d 1565, 1570, 37 USPQ2d 1127, 1132 (Fed. Cir. 1995); In re Wright, 343 F.2d 761, 769-70, 145 USPQ 182, 190 (CCPA 1965).

Acovic and Fried, as discussed above, are totally silent with regard to the width of floating gates 22 and 115, respectively. Claim 6, in contrast, recites that each of the first and second spacers has a width ranging from about 100 Å to about 500 Å. Appellants assert that since neither reference discloses any width or range of widths associated with its respective floating gate, neither reference, singly or in combination can be fairly construed to suggest the range recited in claim 6.

Appellants also note that In re Aller involves determining whether making changes to a temperature range or changes to an acid concentration would be obvious. In re Aller at 235. Acovic and Fried, however, do not disclose any working range or value associated with the width of the floating gates. Therefore, Appellants assert that the determination in In re Aller regarding changes from one particular temperature and acid concentration to another temperature and acid concentration recited in a claim is not on point since Acovic and Fried do not disclose any values for the width of the floating gates. Therefore, Appellants assert that the allegation the claimed range would be obvious based on Acovic and Fried is based on mere speculation. Such speculation does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, the combination of Acovic and Fried does not disclose or suggest each of the features of claim 6. Accordingly, reversal of the rejection of claims 6 and 17 is respectfully requested.

3. Claim 9

Claim 9 recites that the fin structure has a width ranging from about 100 Å to about 1000 Å. The Final Office Action admits that neither Acovic nor Fried discloses this feature, but states that such a feature would be obvious and relies on In re Aller for support (Final Office Action – pages 3-4). Appellants respectfully disagree.

Acovic is totally silent with respect to the width of structure 12. Fried is also totally silent with respect to fin 100. Once again, Appellants assert that absent some disclosure in Acovic or Fried with respect to the width of structure 12 or 100, the combination of Acovic and Fried cannot be fairly construed to suggest that structure 12 or 100 has a width ranging from about 100 Å to about 1000 Å, as required by claim 9.

In addition, similar to the discussion above with respect to claim 6, Appellants assert that reliance on In re Aller and In re Woodruff to somehow render the specifically recited feature of claim 9 as being obvious does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, the combination of Acovic and Fried does not disclose or suggest each of the features of claim 9. Accordingly, reversal of the rejection of claim 9 is respectfully requested.

4. Claims 21 and 22

Claim 21 recites a memory device that includes a first spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the first side surface of the fin structure, the first spacer acting as a first floating gate for the memory device. Claim 21 also recites a second spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the second side surface of the fin structure, the second spacer acting as a second floating gate for the memory device. As discussed above with respect to claim 6, the combination of Acovic and Fried does not disclose or suggest these features. In contrast, Acovic and Fried are totally silent with respect to the width of floating gate 22 and 115, respectively. The Final Office Action admits that the combination of Acovic and Fried does not disclose these features, but once again relies upon In re Aller as providing support for the notion that the claimed ranges would be obvious. Similar to the discussion above with respect to claim 6, Appellants assert that reliance on In re Aller to somehow render the specifically recited features of claim 21 as being obvious does not satisfy the requirements of 35 U.S.C. § 103.

Claim 21 also recites a first gate contacting the insulating layer and disposed on a first side of the fin structure and a second gate contacting the insulating layer and disposed on a second side of the fin structure opposite the first side, wherein the first and second gates are electrically isolated from each other. Similar to the discussion above with respect to claim 1, Appellants assert that the combination of Acovic and Fried cannot be fairly construed to disclose or suggest these features.

For at least the reasons discussed above, Appellants assert that the combination of Acovic and Fried cannot be fairly construed to disclose or suggest each of the features of claim 21.

In addition, even if, for the sake of argument, the combination of Acovic and Fried could be fairly construed to disclose or suggest each of the features of claim 21, Appellants assert that that the motivation to combine Acovic and Fried does not satisfy the requirements of 35 U.S.C. § 103.

For example, the Final Office Action states that it would have been obvious to one of ordinary skill in the art to modify the device of Acovic "by having the control gate to contact the insulating layer for electrical isolation from other surrounding structures as taught by Fried" (Final Office Action – page 5). Appellants note that no portion of either reference is pointed to as providing objective motivation for the combination. Appellants further note that the alleged motivation for combining these disclosures is merely a conclusory statement providing an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 21 under 35 U.S.C. § 103 based on Acovic and Fried is improper. Accordingly, reversal of the rejection of claims 21 and 22 is respectfully requested.

VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-9, 14 and 17-22.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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IX. APPENDIX

1. A memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin structure formed on the insulating layer, the fin structure having a first and second side surface and a top surface;

a dielectric cap formed over the top surface of the fin structure;

a first spacer formed adjacent the first side surface, the first spacer acting as a first floating gate for the memory device;

a second spacer formed adjacent the second side surface, the second spacer acting as a second floating gate for the memory device;

a gate dielectric layer formed on the first and second spacers and over the dielectric cap, the gate dielectric layer contacting the insulating layer and acting as an inter-gate dielectric for the memory device;

a first gate contacting the insulating layer and disposed on a first side of the fin; and

a second gate contacting the insulating layer and disposed on a second side of the fin opposite the first side, wherein the first and second gates are electrically isolated from each other.

2. The memory device of claim 1, further comprising:

a source region and a drain region formed on the insulating layer and disposed adjacent a respective first and second end of the fin structure.

3. The memory device of claim 2, further comprising:

an oxide layer formed on the first and second side surfaces of the fin, the oxide layer acting as a tunnel oxide layer for the memory device.

4. The memory device of claim 3, wherein the oxide layer has a width ranging from about 10 Å to about 100 Å.

5. The memory device of claim 1, wherein the first and second gates are associated with corresponding memory cells that are programmed independently of each other.

6. The memory device of claim 1, wherein each of the first and second spacers comprise polysilicon and have a width ranging from about 100 Å to about 500 Å.

7. The memory device of claim 1, wherein the dielectric cap comprises at least one of a nitride and an oxide.

8. The memory device of claim 1, wherein the insulating layer comprises a buried oxide layer and the fin structure comprises at least one of silicon and germanium.

9. The memory device of claim 8, wherein the fin structure has a width ranging from about 100 Å to about 1000 Å.

14. A non-volatile memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having first and second side surfaces and a top surface;

an oxide layer formed on the first and second side surfaces of the conductive fin;

a dielectric cap formed on the top surface of the conductive fin;

a first spacer formed adjacent the first side surface of the fin, the first spacer acting as a first floating gate electrode;

a first gate formed on the insulating layer, the first gate acting as a first control gate for the non-volatile memory device;

a second spacer formed adjacent the second side surface of the fin, the second spacer acting as a second floating gate electrode;

a second gate formed on the insulating layer, the second gate acting as a second control gate for the non-volatile memory device, wherein the first and second gates are formed on opposite sides of the conductive fin and are electrically isolated from each other; and

an inter-gate dielectric formed between the first spacer and the first gate, between the second spacer and the second gate and over the dielectric cap, wherein the inter-gate dielectric contacts the insulating layer.

17. The non-volatile memory device of claim 14, wherein the first and second spacers each comprise polysilicon and have a width ranging from about 100 Å to about 500 Å.

18. The non-volatile memory device of claim 14, wherein the dielectric cap comprises a nitride.

19. The non-volatile memory device of claim 14, wherein the oxide layer acts as a tunnel oxide for the memory device and the width of the oxide layer ranges from about 10 Å to about 100 Å.

20. The non-volatile memory device of claim 14, wherein the insulating layer comprises a buried oxide layer and the conductive fin comprises at least one of silicon and germanium.

21. A memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin structure formed on the insulating layer, the fin structure having a first and second side surface and a top surface;

an oxide layer having a width ranging from about 10 Å to about 100 Å formed on the first and second side surfaces of the fin structure, the oxide layer acting as a tunnel oxide layer for the memory device;

a first spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the first side surface of the fin structure, the first spacer acting as a first floating gate for the memory device;

a second spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the second side surface of the fin structure, the second spacer acting as a second floating gate for the memory device;

a gate dielectric layer formed on the first and second spacers and over the top surface of the fin structure;

a first gate contacting the insulating layer and disposed on a first side of the fin structure;

a second gate contacting the insulating layer and disposed on a second side of the fin structure opposite the first side, wherein the first and second gates are electrically isolated from each other;

a source region formed on the insulating layer adjacent a first end of the fin structure; and

a drain region formed on the insulating layer adjacent a second end of the fin structure opposite the first end.

22. The memory device of claim 21, wherein the gate dielectric comprises an oxide having a thickness ranging from about 50 Å to about 200 Å.

X. EVIDENCE APPENDIX

None

XI. RELATED PROCEEDINGS APPENDIX

None